1. How Does PC Diagnostic Cards Works?

When a computer power on it goes on POST(Power On Self Test) first. It will check the circuit system, memory, keyboard, video, hard drives, floppy drives etc., and analyze the hard disk system configurations and initialize I/O system. And then it will boot the O/P if each part is normal, or it will fail to boot. The salient feature is the appearance of the cursor. The computer will the key components before you see the cursor. If there are faults with the key components, the system will halt,and you will see nothing. And then it will go on checking the non-key-components, the system will boot even if there are faults, such as the monitor shows nothing. Under this circumstance, plug the card in the PCI or ISA slot,with help the accompanied manual you will find the fault components easily.

PC Diagnostic Card(PC Analyzer) is a tool that shows all the POST codes. When there is fault, it will halt and you will see the code on card. Look up the code in the accompanied manual and you will know which part of your computer has gone wrong.

It greatly reduces the guesswork, especially, when the screen is blank, O/S can not boot, or speaker does not work.

2. Function of Indicator Lights

- CLK - Bus Clock, constantly lights on, normal;
- IRDY - It is on when there is IRDY signal, or it is off;
- Frame - constantly lights on.
- RST - Lights on for a half second then goes out, normal.

A. Conditions of POST CODES "00" and "FF"

1) If "00" or "FF" come after a series of other codes, motherboard is okay;

2) If CMOS is setting up okay, non-serious error won't stop POST, finally the card will show "00" or "FF";

3) If the card shows "00", "FF" or other initial codes when power on, the motherboard does not work.

B. The codes in the table are listed by a sequence of the number, from small to large, and this does not mean the codes showed in testing will follow this sequence.

C. The codes that the BIOS supplier gives no definition are not listed in this table.

D. The same BIOS Code means differently by different bios supplier(like AMI, AWARD, PHOENIX).

You have make sure which kind of bios your computer is using now. You may find it from your computer manual or the chip of the motherboard.

E. There are few motherbaords that only part of the codes are sent from the PCI slot, but the ISA slot will send all the codes to the card.

Till now we have found that there is individual original computer that there is no codes sent to the card from ISA slot. PCI slot sends all the codes.

So we suggest that you try both PCI and ISA slot when the card shows no codes. In additional,

we want to point out that PCI slots on the same motherboard may work differently, part of them send codes to the card while others not, take Dell 810 motherboard for example, the PCI slot nearest to CPU will show all the codes and stop at "00" or "FF," while other slots stop at "38".

F. Time for Reset may be different to ISA slot and PCI slot. Probably there is such condition that ISA slot start to send codes while PCI Reset Indicator has not gone out yet.

3. Functional Characteristics

1. There is no need to install software. Combining advanced technology and user's behavioral science, YUQUAN Electronics Co., Ltd humanized PC Diagnostic Card to be user-friendly. it is very easy to use. Thus it is not only applicable to the technicians, but also general PC users. It will make all new users professional masters.

2. Using large-scale IC integrated module with compact structure and stable performance, With more internal resources, it has more excellent anti-jamming performance and lower rate of self failures.
3. Functional limitation of traditional PC Diagnostic Cards has been broken, e.g. we have created standard PCI interface and varieties of auxiliary parts that enhance the accuracy and reliability of PC Diagnostic Cards. And part of its functions depend on BIOS no more, and never limit to POST contents and manners.
4. Unlike traditional PC diagnostic cards that become useless when the system booted, The NEW PC Diagnostic Cards helps you solve problems like system halt, blank screen, and instability, and keeps your computer running safely and stably.
5. Unprecedented compatibility. The Cards are compatible with all kinds of high, middle and low classes of motherboards in the market, and shows more accurate failure codes, there is even no exception for Intel 9XX series that represent the mainstream of top motherboards (such as SIS671) which can not be tested by the traditional PC diagnostic card.
6. The random initial codes which mislead the diagnoses are thoroughly eliminated. Diagnostic Card no more depends on RESET signal of the test computer, and can prevent impulse loss, correct failures automatically, even if the reset logic of the test computer is abnormal, it will not influence the testing functions of Diagnostics Cards and New Generation PC Diagnostic Card.
7. Adopting excellent control algorithm to page down the codes, which is easier than the traditional diagnostic cards do, PC Diagnostic Cards greatly lower the rate of inappropriate operation that lead to a low accuracy in test.
8. All the indicator lamps (such as CLK, IRDY and FRAME) are 100% correct. They will be ON only when there are signals and OFF when there are no signals, while the traditional ones will be ON once they have signals. Take the CLK indicator for example, it makes the users see clearly even single 10ns impulse. It will not be on when there is no CLK signal impulse, no matter the current signal stays at high or low level, which won't mislead the user. No pulse loss, and no useless pulse.
9. The Diagnostics Cards are even more advanced than the New Generation PC Diagnostic Cards. They extremely eliminated wrong codes, redundant codes, and won't miss any needed codes. The users can check all the failure codes by check switch. They are really the most accurate all around the world.
10. Eliminated the fault that test stops halfway, which makes test more efficient and reliable.
11. Supports 80h, 84h and 300h ports.

4. How to Install PC Diagnostic Cards

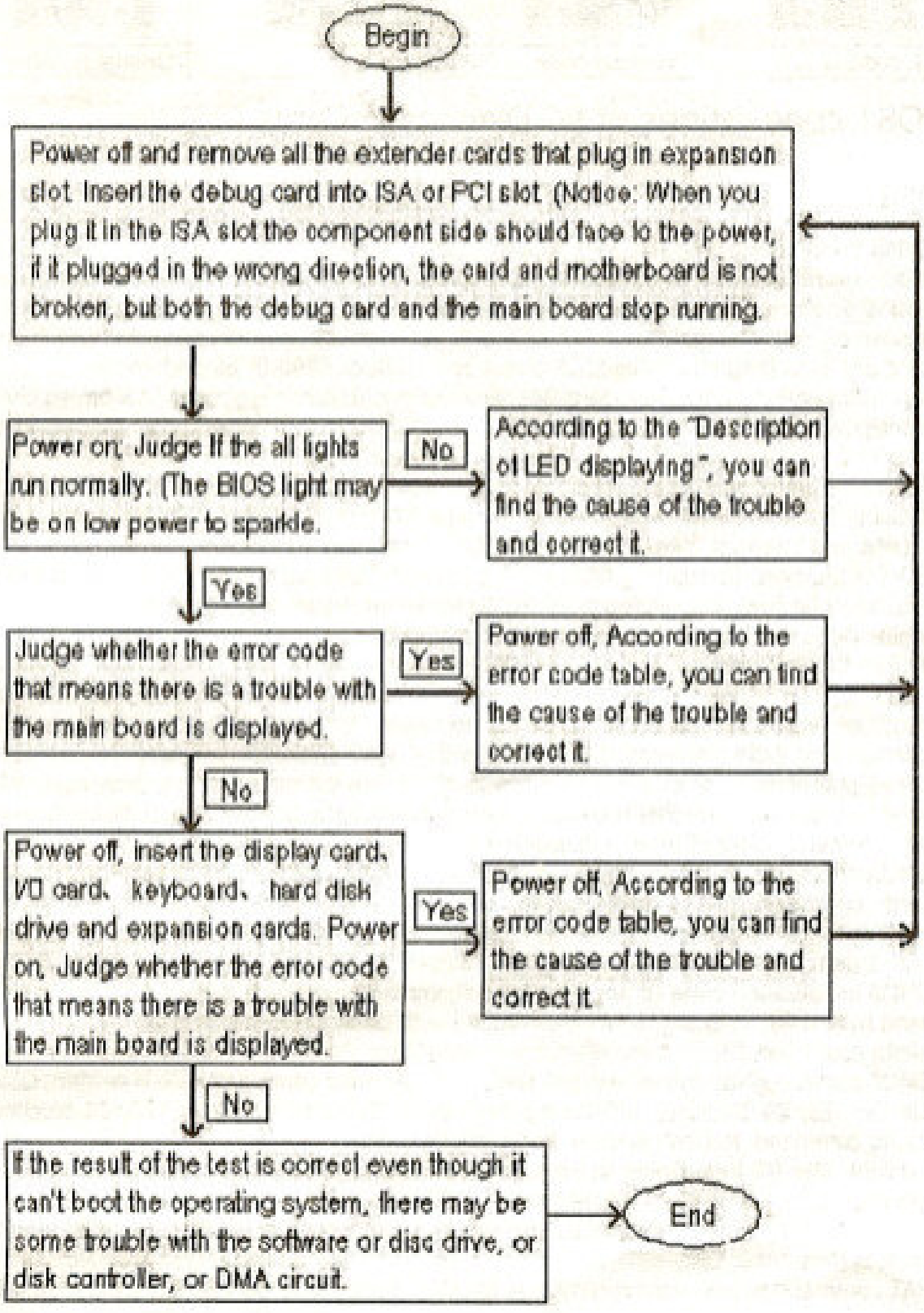
To install PC Diagnostic Cards, you must switch power to the computer off, plug it into any ISA,EISA, or PCI bus slot, and switch power back on. If all the slots are full, you will have to remove a card. We recommend not removing the video card because it is needed to show information on the system display. You can identify an ISA or EISA slot because its edge connector has wider pins than a PCI slot. You should install the card so the component side of the board faces the power supply and the right-hand edge aims to the rear of the computer. The PCI edge of the card has a key slot that prevents you from installing the card backward. However, it is possible to install the card backward in an ISA slot. If you install it backward, protection components on PC Diagnostic Cards prevent it from burning out immediately, but the card will not function, and you should immediately switch power off and install the card facing the opposite direction. Your warranty will be voided if you damage the card by plugging it in backward.

PC Diagnostic Cards will not show POST codes in systems that does not emit POST codes to port 80 or 680, including the IBM PC, early Hewlett Packard Vectras, and systems with AMI-XT BIOS, ERSO BIOS, or DTK BIOS.

5. What A POST Card Won't Do

A typical POST card is passive, and it will not:
Actively test the computer (it is a passive device); show POST results on its display better than system BIOS allows; measure signal timing or relationships; find ALL computer problems, especially those that cannot be detected BEFORE the system boots (such as bad sectors on hard drives, software/hardware incompatibilities, and detailed hardware errors that are not detected by the system BIOS' POST.

6. PC Diagnostic Cards Flow Chart Operating Guide



While the PC Diagnostic Cards is testing the mainboard, the tens digit and the units digit show the POST code that is previous to the POST code of thousands digit and the hundreds digit; While You use the function switch to thumb through the POST codes, the tens digit and the units digit show count number of the POST codes that is the make up of thousands digit and the hundreds. (The PC Diagnostic Cards can memorize 48 POST codes. The count number is from 00 to 47 .)

While Testing automatically:				While thumbing through codes:			
thousands	hundreds	tens	units	thousands	hundreds	tens	units
digit	digit	digit	digit	digit	digit	digit	digit
							
POST code		Previous code		POST code		Ordinal number	

7. POST code listings of PC Diagnostic Cards

(1) AMI

(00) Going to give control to INT 19H boot loader.
(10) Processor register test about to start, and NMI to be disabled,286 reg. test about to start.
(02) NMI is disabled. Power on delay starting. Power on de- lay starting.286reg.
(03) Power on delay complete. To check so ft reset/power -on. Any initialization before keyboard BAT is in progress. ROM BIOS check sum (32K at F800:0) passed.
(04) Any initialization before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset/power-on. Reading keyboard SYS bit, to check soft reset/power on. Keyboard controller test with and without mouse passed. 8259 initialization OK.
(05) Soft reset/power -on determined. Going to enable ROM. i.e. disable shadow RAM/Cache if any. Going to enable ROM, .i.e. disable shadow RAM/cache if any. Chipset initialization over, DMA and interrupt controller disabled. CMOS pending interrupt disabled.
(06) ROM is enabled. Calculating ROM BIOS checksum, and waiting for Keyboard controller input buffer to be free. Calculating ROM BIOS checksum. Video disabled and sys- tem timer test begin. Video disabled and system timer counting OK.
(07) ROM BIOS checksum passed .CMOS shutdown register test to be done next. ROM BIOS checksum passed, Keyboard controller I/B free. Going to issue the BAT command to keyboard controller. Going to issue the BAT command to keyboard controller.CH-2 of 8254 initialization half way.CH-2 of 8253 test OK.
(08) CMOS shutdown register test done. CMOS checksum calculation to be done next. BAT command to keyboard controller is issued. Going to verify the BAT command. Going to verify the BAT command. CH-2 of timer initialization over. CH-2 delta count test OK.
(09) CMOS checksum calculation is done, CMOS diag byte written. CMOS initialize to begin. Keyboard controller BAT result verified. Keyboard command byte to be written next.(09)Keyboard command byte to be written next. CH -1 of timer initialization o ver. CH-1 delta count test OK.
(0A) CMOS initialization done (if any). Keyboard command byte code is issued. Going to write command byte data. Going to write command byte data. CH -0 of timer initialization over. CH-0 delta count test OK.
(0B) CMOS status register initialize done. Keyboard controller command byte is written. Going to issue Pin -23, 24 blocking/ unblocking co mmand. Going to issue pin -23, 24 blocking/ unblocking command. Refresh started. Parity status cleared.
(0C) KB controller I/B free. Going to issue the BAT command to keyboard controller. Pin-3,24 of keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next. NOP command of keyboard controller to be issued next. System timer started. Refresh & system timer OK.
(0D) BAT command to keyboard controller is issued. Going to verify the BAT command. NOP

command processing is done. CMOS shutdown register test to be done next. CMOS shutdown register test to be done next. Refresh link toggling passed. Refresh link toggling passed.
(0E) Keyboard controller BAT result verified. Any initialization after KB controller BAT to be next. CMOS shut down register R/W test passed. Going to calculate CMOS checksum, and update DIAG. Going to calculate CMOS checks um, and update DIAG Byte. Refresh period ON/OFF 50% OK.
(0F) initialization after KB controller BAT done. Keyboard command byte to be written next. CMOS checksum calculation is done, DIAG byte written. CMOS Init. To begin (If "INIT C MOS IN EVERY BOOT IS SET"). CMOS initialization to begin (If "INIT CMOS IN E VERY BOOT IS SET").
(10) KB controller command byte is written. Going to issue p in-23,24 blocking/unblocking command. CMOS initialization done (if any). CMOS status register about to Init for Date and Time. CMOS status register about to Init for Date and Time. Refresh on and about to start 64K base memory test. Confirmed refresh ON & about to start 64 K memory.
(11) Pin23,24 of keyboard controller is blocked/unblocked. Going to check to check pressing of <INS>key during power-on. CMOS status register initialized. Going to disable DMA and Interrupt controllers. Going to disable DMA and interrupt controllers. Address line test passed. Address line test passed.
(12) Checking for pressing of <INS> key during power-on done. Going to disable DMA and Interrupt controllers. D MA controller#1,#2,interrupt controller#1,#2 disabled. About to disable Video display and Init port -B. About to disable video display and Init port -B.64K base memory test passed. 64K base memory test passed.
(13) DMA controller#1,#2 ,interrupt controller#1,#2disa- bled. About to disable
Video display and initialize port -B. Chipset initialize/auto memory detection about to begin. Replace first memory SIMM.(13)Chipset initialize/auto memory detection about to begin. Check first SIMM.(13) Interrupt vectors initialized.
(14) Chipset initializatjon/auto memory detection over. To uncompress the POST code if compressed BIOS. 8254 timer test about to start. 8254 timer test about to start.8042 keyboard controller test OK.
(15) POST code is un -compressed.8254 timer about to start. CH-2 timer test halfway. 8254 CH-2 timer test to be completed. 8254 CH-2 timer test to be completed. Interrupt vectors initialized. CMOS read/write test OK.
(16) CH-2 timer test over.8254 CH-1 timer test to be completed. CMOS checksum/battery check OK.
(17) CH-1 timer test over. 8254 CH-0 timer test to be completed. Monochrome mode set.
(18) CH-0 timer test over. About to start memory refresh. Color mode set.
(19) 82 timer test over. Memory refresh test tobe done next. About to look for optional video ROM at segment C000 and give control to the optional video ROM if
present.
(1A) Memory refresh line is toggling. Going to check 15 micro second ON/OFF time. Return from optional video ROM. Optional video ROM control OK
(1B) Memory refresh period 30 micro second test complete. Base 64K memory test about to start. Shadow RAM enable /disable completed. Display memory
read/write test OK.
(1C) Display memory read/write test for main display type as set in the CMOS
setup program over. Display memory read/write test for alternate display OK.
(1D) Display memory read/write test for alternate display type complete if main display memory read/write test returns error. Video retrace check OK. Set configuration from CMOS.
(1E) Global equipment byte set for proper display type.
(1F) Video mode set call for mono/color be gins.'Mode set call for mono/color OK. Set EISA mode; If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA test an clear EISA mode flag. Test EISA configuration memory integrity (checksum & communication interface).

(20) Memory refreshes period 30 micro second test complete. Base 64K memory/address test started. Address line test to be done next. Video mode set completed.
(21) Address line test passed. Going to do toggle parity. ROM type 27256 verified. Video display OK.
(22) Toggle parity over. Going for sequential data R/W test on 64 K memory. Power on message display OK.
(23) Base 64K sequential data R/W test passed. Going to SET BIOS stack and to do any setup before Interrupt vector Init. Any setup before interrupt vector Init about to start. Power on message displayed.
(24) Setup required before vector initialization complete. Interrupt vector initialization about to begin.
(25) Interrupt vector initialization done. Going to read Input port of 9042 for turbo switch (if any).Going to read I/O port of 8042 for turbo switch (if any).
(26) I/O port of 8042 is read. Going to initialize global data for turbo switch. Going to initialize global data for turbo switch.
(27) Global data initialization for turbo switch is over. Any initialization before setting video mode to be done next.
(28) Initialization before setting video mode is complete. Going for monochrome mode and color setting. Check extended memory.
(29) Monochrome mode setting is done. Going for color mode setting.
(2A) Monochrome Color mode setting is done. About to go for toggle parity before optional ROM test. About to go for toggle parity before optional ROM Check.
(2B) Toggle parity over. About to give control for any setup required before optional video ROM check.
(2C) Processing before video ROM control is done. About to look for optional video ROM and give control.
(2D) Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
(2E) Return from processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
(2F) EGA/VGA not found. Display memory R/W test about to begin.
(30) Display memory R/W test passed. About to look for the retrace checking. Virtual mode memory test about to begin.
(31) Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test. Virtual mode memory test started.
(32) Alternate display memory R/W test passed. About to look for the alternate display retrace checking. Processor executing in virtual mode.
(33) Video display checking over. Verification of display type with switch setting and actual card to begin. Verification of display type with switch setting and Actual Card to begin. Memory address line test in progress.
(34)Verification of display adapter done. Display mode to be set next. Memory address line test in progress.
(35) Display mode set complete. BIOS ROM data area about to be checked. Memory below 1MB calculated.
(36) BIOS ROM data area check over. Going to set cursor for power on message. Memory above 1MB calculated.
(37) Cursor setting for power on message id complete. Going to display the power on message. Memory test about to start.
(38) Power on message display complete. Going to read new cursor position. Memory below 1MB initialized.
(39) New cursor position read and saved. Going go display the Hit< DEL>message. Memory above 1MB initialized.
(3A) Check memories, first 64K, one long beep. Reference string display is over. Going to display the Hit<ESC> massage. Memory size display initiated. This will be updated

when the BIOS goes through the memory. Award (3A) Check memory.
(3B) Hit<DEL>or<ESC>message displayed. Virtual mode memory test about to start, About to start below 1MB memory test.
(3C) Memory test below 1MB completed and about to start above 1MB test. Award (3C) Set flag to allow users to enter CMOS setup utility. Setup enabled.
Phoenix (3C)Configure advanced chipset registers.(Beep)=1 -4-4-1. Determine relative CPU speed.
(3D) Memory test above 1MB completed.
(3E) About to go to real mode (shutdown).
(3F) Shutdown successful and Processor in real mode.
(40) Preparation for virtual mode test started. Going to verify from video memory. CACHE memory on and about to disable A20 address line.
(41) Returned after verifying from display memory. Going to prepare the descriptor babbles. A20 address line disabled successful.
(42) Descriptor tables prepared. Going to enter in virtual mode for memory test. 486 internal cache turned on. About to start DMA controller test.
(43) Entered in the virtual mode. Going to enable interrupts for diagnostics mode. About to start DMA controller test.
(44) Interrupts enabled (if post switch is on). Going to initialize data to check memory wrap around at 0:0.
(45) Data initialized. Going to check for memory wrap around at 0:0 and the total system memory size.
(46) Memory wrap around test done. Memory size calculation over, writing pat terns to test memory.
(47) Pattern to be tested written in extended memory, 640 K memory.
(48) Patterns written in base memory. Going to find out amount of memory below 1M memory.
(49) Memory below 1M found and verified. Going to find out amount of memory above 1M memory.
(4A) Amount of memory above 1M found and verified. Going for BIOS ROM data area check.
(4B) Amount o f memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for reset (If power on, go to check point#4Eh).
BIOS ROM data areas check over. Going to check <ESC> and to clear memory below 1M for soft reset.
(4C) Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
(4D) Memory above 1M cleared. (SOFT RESET) Going to save the memory size.(GOTO check point#52h).
(4E) Memory test started. (NO SOFT RESET) About to display the first 64K memory test.
(4F) Memory size display started. This will be updated during memory test. Going for sequential and random memory test. Processor in real mode after shutdown.
(50) Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation /shadow. DMA page register test complete.
(51) Memory size display adjusted due to relocation/shadow. Memory test above 1M to follow. DMA unit -1 base register test about to start.
(52) Memory testing/initialization below 1M complete. Going to save memory size information. Going to prepare to go back to real mode. DMA un it-1 channel OK,about to begin CH-2.
(53) Memory size information is saved. CPU registers are saved. Going to enter in real mode. DMA CH-2 base register test OK.
(54) Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shut down. About to check F/F latch for unit-1 and unit-2.
(55) Registers restored. Going to disable gate A20 address line. F/F latch for both units checked.
(56) A20 address line disable successful. BIOS ROM data area about to be checked. DMA unit 1 and 2 programming over and about to initialize 8259 interrupt controller.

(57) A20 address line disable successful. BIOS ROM data area check halfway. BIOS ROM data area check to be com plete.8259 initialization over.
(58) Memory size adjusted for relocation/shadow. Going to clear Hit<DEL>message. BIOS ROM data area check over. Going to clear Hit<ESC> message.
8259 mask register check OK.
(59) Hit<ESC>message cleared. <Wait..>message displayed. About to start DMA and interrupt controller test. Master 8259 mask register OK, about to start slave.
(5A) About to check timer and keyboard interrupt level.
(5B) Timer interrupt OK.
(5C) About to test keyboard interrupt.
(5D) ERROR! Timer/keyboard interrupt not in proper level.
(5E) 8259 interrupt controller error.
(5F) 8259 interrupt controller test OK.
(60) DMA page register test passed. About to go for DMA #1, verify from display memory.
(61) Display memory verification over. About to go for DMA #1 base register test.
(62) DMA#1 base register test passed. About to go for DMA #2 base register test.
(63) DMA #2 base register test passed. About to go for BIOS ROM data area check.
(64) BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
(65) DMA #2 base register test passed. About to program DMA unit 1 and 2.
(66) DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
(67) 8259 initialization over. About To start keyboard test.
(70) Start of keyboard test.
(71) Keyboard controller BAT test over.
(72) Keyboard interface test over, mouse interface test started.
(73) Global data initialization for keyboard/mouse over.
(74) Display 'SETUP' prompt and about to start floppy setup.
(75) Floppy setup over.
(76) Hard disk setup about to start.
(77) Hard disk setup over.
(79) About to initialize timer data area.
(7A) Timer data initialized and about to verify CMOS batter y power.
(7B) CMOS batter y verification over.
(7D) About to analyze POST results. About to analyze diagnostic test results for memory.
(7E) CMOS memory size updated.
(7F) Look for <DEL> key and get into CMOS setup if found. About to check optional ROM C000:0.
(80) Keyboard test started, clearing output buffer, checking for stuck key, About to issue keyboard reset command. About to give control to optional ROM in segment
C800 to DE00.
(81) Keyboard reset error/stuck key found. About to issue keyboard controller interface test command. Optional ROM control over.
(82) Keyboard controller interface test over. About to write command byte and Init circular buffer. Check for printer ports and put the addresses in global data area.
(83) Command byte written, global data Init done. About to check for lock -key. Check for RS232 ports and put the addresses in global data area.
(83) Command byte written, global data Init done. About to check for lock -key. Check for RS232 ports and put the addresses in global data area.
(84) Lock-key checking over. About to check for memory size mismatch with CMOS. Co-Processor detection over. 80287 check/test OK.
(85) Memory size check done. About to display soft error and check for password or bypass setup. About to display soft error message. If no video replace Video card.
(86) Password checked. About to do programming before setup. About to give control to system ROM at segment E000.
(87) Programming before setup complete. Going to uncompress SETUP code and execute

CMOS setup. System ROM E000:0 check over.
(88) Returned from CMOS setup program and screen is cleared. About to do programming after setup.
(89) Programming after setup complete. Going to display power on screen message.
(8A) First screen message displayed. About to display <WAIT...>message.
(8B) First screen message displayed <WAIT...> message displayed. About to do Main and Video BIOS shadow.
(8C) Main and video BIOS shadow successful. Setup options programming after CMOS setup about to start.
(8D) Setup options are programmed, mouse check and Init to be done next. Going for hard disk, floppy reset.
(8E) Mouse check and initialization complete. Goirg for hard disk controller reset. About to go For floppy check.
(8F) Hard disk controller reset done. Floppy setup to be done nest.
(90) Floppy setup is over. Test for hard disk presence to be done.
(91) Floppy setup complete. Hard disk setup to be done next.
(92) Hard disk setup complete. About to go for BIOS ROM data area check.
(93) BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
(94) Hard disk setup complete. Going to set base and extended memory size. BIOS ROM data area check over.
(95) Memory size adjusted due to mouse support, hard disk type-47. Going to verify from display memory.
(96) Memory size adjusted due to mouse support, hard disk type -47.Going to do any Init before C800 optical ROM control. Returned after verifying from display memory.
(97) Any Init before C800 optional ROM control is over. Optional ROM check & control will be done next.
(98) Optional ROM control is done. About to givecontrol to do any required processing after optional ROM returns control.
(99) Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
(9A) Return after setting timer and printer base address. Going to set the RS -232 base address.
(9B) Returned after RS-232 base address. Goirg to de any initialization before Co-Processor test.
(9C) Required initialization before Co-Processor is over. Going to initialize the Co-Processor next.
(9D) Co-Processor initialized. Going to do any initialization after Co-Processor test.
(9E) Initialization after Co-Processor test is completed. Going to check expander keyboard, keyboard ID and number-lock.
(9F) Extended keyboard check is done, ID flag set. Number-lock on/off. Keyboard ID command to be issued.
(A0) Keyboard ID command issued. Keyboard ID flag to be reset. Compaq (A0) Start of diskette tests.
(A1) Keyboard ID flag reset. Cache memory test to follow.
(A2) Cache memory test over. Going to display any soft errors.
(A3) Soft error display complete. Going to set the keyboard type matric rate.
(A4) Keyboard type matric rate set. Going to program memory wait states.
(A5) Memory waits states programming over. Going to clear the screen and enable parity/NMI.
(A6) Screen cleared. Going to enable parity and NMI.
(A7) NMI and parity enabled. Going to do any Initialization required before giving control to optional ROM at E000.
(A8) Initialization before E0 00 ROM control over. E000 ROM to get control next.
(A9) Returned from E000 ROM control. Going to do any init required after E000 optional ROM

control.
(AA) Initialization after E000 optional ROM control is over. Going to display the system configuration.
(B0) System configuration is displayed. Going to un-com-press SETUP code for hot-key setup.
(B1) Un-compressing of SETUP code is complete. Going to copy any code to specific area.
(C2) NMI is Disable. Power on delay start on.
(C3) Check memory (Cache, Video or first 64 K).
(C5) Power on delay complete. Going to enable ROM i.c. disable Cache if any.
(C6) Calculating ROM BIOS checksum.
(C7) ROM BIOS checksum passed. CMOS shutdown register test to be done next.
(C8) CMOS shut down register test done. CMOS checksum calculation to be done next.
(CA) CMOS checksum calculation is done, CMOS Drag byte written. CMOS status register about to initializing for Date and Time.
(CB)CMOS status register Init done. Any initialization before keyboard BAT to be done next.
(CD) BAT command to keyboard controller is to be issued.
(CE) Keyboard controller BAT result verified. Any initialization after KB controller.
(CF) Initialization after KB controller BAT done. Keyboard command byte to be written next.
(D1) Keyboard controller command byte is written. Going to check pressing of <INS> key during power-on.
(D2) Checking for pressing of <INS>key during power-on done. Going to disable DMA and Interrupt controllers.
(D3) DMA controller #1, #2, interrupt controller #1, #2 disable. Video display is disable and port-B is initialized. Chipset initialize/auto memory detection about to begin.
(D4) Chipset Initialization/auto memory detection about to begin. Check SIMM for mismatch.
(D5) RUNT IME code is un-compressed.
(DD) Transfer control to uncompressed code in shadow ram at F000:FFF0.

(2) AWARD

(01) Processor test 1; Processor status (1FLAGS) verification; Tests the following processor status flags carry, zero, sign, overflow. The BIOS will set each of these flags, verify they are set then turn each flag off and verify it is off.
(02) Processor test 2; Read/write/verify all CPU registers except SS, SP and BP with data pattern FF&00. Determine status of manufacturing jumper.
(03) Initialize Chips; Disable NMI, PIE, AIE, UEI, SQWV, disable video, parity checking, DMA; Reset math Coprocessor; Clear all page registers, CMOS shutdown byte; Initialize timer 0, 1 and 2 including set EISA timer to a known state; Initialize DMA controllers 0 and 1; Initialize interrupt controller 0 and 1; Initialize EISA extended registers. Calculate BIOS EPROM and sign -on message checksum; fail if not 0. Initialize EISA registers (EISA) BIOS only. Clear 8042 keyboard controller.
(04) Test memory refresh toggle; RAM must be periodically refreshed in order to keep the memory from decaying. This function assures that the memory refresh function is working properly. Test CMOS RAM I/O port interface and verify battery power is available (bat. status=1). Reset 8042.
(05) Keyboard controller self-test enable keyboard inter face. Blank video, Initialize keyboard; Keyboard controller initialization. Initialize Chips; Disable NMI, PIE, AIE, UEI, SQWV, disable video, parity checking, DMA; Reset math Coprocessor; Clear all page registers, CMOS shutdown byte; Initialize timer 0, 1 and 2 including set EISA timer to a known state; Initialize DMA controllers 0 and 1; Initialize interrupt controller 0 an d 1; Initialize EISA extended Registers. Get
manufacturing status, reset if set(loop 1 -5).
(06) Test memory refresh toggle; RAM must be periodically refreshed in order to keep the memory from decaying. This function assures that the memory refresh function is working properly. Initialize chips.
(07) Verifies CMOS's basis R/W functionality. Test CMOS interface and battery status;

Verifies CMOS is working correctly, detects bad battery. Setup low memory; Early chip set initialization; Memory presence test; OEM chip set routines; Clear low 64K of memory; Test first 64 K memory; clear lower 256K of memory, enable parity checking and test parity in lower 256K; test lower 25 If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays 6K memory. Set up stack, beep. Read/write/verify CPU registers.

(08) Setup low memory; Early chip set initialization; Memory presence test; OEM chip set routines; Clear low 64K of memory; Test first 64K memory; clear lower 256K of memory, enable parity checking and test parity in lower 256K; test lower 256K memory. Set up stack, beep. Setup interrupt vector table in lower 1K RAM area; Initialize first 120 interrupt vectors with SPURIOUS_INT_HD LR and initialize INT 00h-1Fh according to INT_TBL. Initialize CMOS timer.

(09) Program the configuration register of Cyrix CPU. OEM specific cache initialization. Early Cache initialization; Cyrix CPU initialization; cache initialization.

Test CMOS RAM checksum; beep; also test extended storage of parameters in the motherboard chipset; if not warm- booting; display the Test CMOS RAM checksum message, if bad, or insert key pressed, load defaults if bad. Check BIOS Checksum.

(0A) Initialize the first 32 interrupt vectors. Initialize INTs 33 to 120.Early Power Management initialization. Setup interrupt vector table in lower 1 K RAM area; Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL. Initialize key - board; Detect type of keyboard controller (optional 8242 or 8248, with Ned don XOR gate control); Set NUM_LOCK status. Reset keyboard test keyboard controller interface to verify it returned AAH and responded to enable/disable commands, set keyboard buffer, enable keyboard and keyboard interrupts for normal use, beep, halt. Initialize Video controller.

(0B) Verify the RTC time is valid or not. Detect bad battery. Read CMOS data into BIOS s tack area. Perform PnP initializations. Assign I/O & Memory for PCI devices (PCI BIOS Only). Test CMOS RAM checksum; beep; also test extended storage of parameters in the motherboard chipset; if not warm-booting, display the Test CMOS RAM checksum message, if bad, or insert key pressed, load defaults if bad.

Initialize video interface; Detect CPU clock; Read CMOS location 14b to find out type of video in use; Detect and initialize video adapter. 8254 timer, channel 0 test.

(0C) Initialization of the BIOS data area (40:00 -40:FF). Initialize keyboard; Detect type of keyboard controller (optional 8242 or 8248, with Nedadon XOR gate control); Set NUM_LOCK status. Reset keyboard test keyboard controller interface to verify it returned AAH and responded to enable/disable commands, set keyboard buffer, enable keyboard and keyboard interrupts for normal use, beep, halt. 8254 timer, channel 1 test.

(0D) Program some of the chipset's value. Measure CPU speed for display. Video initialization including MDA, CGA, EGA/VGA. Initialize video interface; Detect CPU clock; Read CMOS location 14b to find out type of video in use; Detect and initialize video adapter. OEM specific-Initialize motherboard special chipset as required by OEM; initialize cache controller early, when cache is separate from chipset.8254 timer, channel 2 test.

(0E) Initialize the APIC(Multi-Processor BIOS only). Test video RAM(If Monochrome display device found). Show startup screen message. Test video memory; Test video memory, write sign-on message to screen. Setup shadow RAM-Enable shadow according to setup. Test COMS Shut down byte.

(0F) DMA channel 0 Test. Test DMA controller 0; BIOS checksum test, keyboard detect and initialization. Test Extended CMOS.

(10) DMA channel 1 Test. Test DMA controller 1 with AA, 55, FF,00 pattern.8237 DMA, channel 0 test.

(11) DMA page register test. Test DMA page registers, use I/O ports to test address circuits. POST enables user reboot here. Test DMA page registers. FATAL DISP LAY ERRORS. 8237 DMA, channel 1 test.

(12) Call support 800 -909-3424. Test 8254 timer 0 channel 0. Test DMA page registers.

(13) Test 8254 timer 0 channel 1. Test keyboard controller.

(14) Test 8254 timer 0 counter 2. Test timer counter 2; Test 8254 timer 0 counter 2. Test memory refresh.
(15) Test 8259 interrupt mask bits for channel 1. Test 8259-1 mask bits; Verify 8259 channel 1 masked interrupt by alternate turning off and on the interrupt line. Test 1st 64K of system memory.
(16) Test 8259-2 mask bits; Verify 8259 channel 2 masked interrupt by alternate turning off and on the interrupt line. Setup Interrupt vectors.
(17) Test struck 8259's interrupt bits; Turn off interrupt then verify no interrupt mask register is on. Setup video I/O operations.
(18) Test 8259 interrupt functionality; Force an interrupt and verify the interrupt occurred. Test video memory.
(19) Test 8259 functionality. Test stuck NON-Maskable Interrupt bits(Parity/I/O check);Verify NMI can be cleared. 8259 Interrupt controller, channel 1 mask bits test.
(1A) Display CPU clock.8259 Interrupt controller, channel 2 mask bits test.
(1B) Test CMOS battery status. Test the system ROM.
(1C)Test CMOS RAM checks um. Test CMOS.
(1E) If EISA NVM checksum is good, execute EISA initialization(EISA BIOS ONLY). Size system memory.
(1F)Test system memory.
(20) Enable slot 0; Initialize slot 0(system board). (Check memory size). 8259 stuck bits test.
(21) Enable slots 1 through 15; Initialize slot 1.Test stuck NMI bits (parity I/O check).
(22) Enable slots 2; Initialize slot 2. Test 8259 working.
(23) Enable slots 3;Initialize slot 3. Test protected mode.
(24) Enable slots 4; Initialize slot 4.Size extended memory.
(25) Enable slots 5; Initialize slot 5. Test extended memory.
(26) Enable slots 6; Initialize slot 6. Test protected mode exceptions.
(27) Enable slots 7; Initialize slot 7. Setup cache control or shadow RAM.
(28) Enable slots 8; Initialize slot 8. Setup 8242.
(29) Enable slots 9; Initialize slot 9.
(2A) Enable slots A; Initialize slot A. (2A)8242 initialization.
(2B) Enable slots B; Initialize slot B. Initialize floppy drive and controller.
(2C) Enable slots C; Initialize slot C. Detect & initialize serial ports.
(2D) Enable slots D; Initialize slot D. Detect & initialize parallel ports. Test timer 2.
(2E) Enable slots E; Initialize slot E. Initialize hard drive & controller.
(2F) Enable slots F; Initialize slot F. Detect & initialize 80x87 Coprocessor.
(30) Get base memory & extended memory size. Size base And extended memory from 256K to 640K and extended memory above 1MB.
(31) Test base and extended memory; Test base memory from 256K to 640K and extended memory above 1MB using various patterns. Detect & initialize optional ROMs.
(32) Display the Award Plug & Play BIOS extension message (PnP BIOS only).Test EISA extended memory; If EISA mode flag is set then test EISA memory found in slots initialization, T his test is skipped in ISA mode and can be skipped with ESC key in EISA mode.
(33) Call Tech Support 727 -532-4151.
(36) Warm Start shut down.
(38) shadow system BIOS ROM.
(3A) Auto size cache.
(3C) Advanced configuration of chipset registers.
(3D) Initialize keyboard. Install PS/2 mouse. Initialize & install mouse; Detect if mouse is present, initialize mouse, install interrupt vectors.
(3E) Try to turn on level 2 cache.
(3F) Enable shadow RAM per CMOS RAM setup or if MEMORY TYPE is SYS in the EISA configuration.
(40) Display virus protest disable or enable.
(41) Initialize floppy disk drive controller.

(42) Initialize hard drive & controller; Initialize hard drive controller and any drives.
(43) If it is a PnP BIOS, initialize serial & parallel ports. Detect & initialize serial/parallel ports; Initialize any serial and parallel ports (also game port).
(44) Going to initialize data to check memory re -map at 0:0.
(45) Detect & Initialize math Coprocessor; Initialize math Coprocessor.
(46) Display the setup message (to press Ctrl -Alt-Esc to enter setup), and enable setup.
(47) Set system speed for boot.
(48) Check video configuration against CMOS.
(49) Initialize PCI bus and devices.
(4A) Initialize all video adapters in system.
(4B) QuietBoot start (optional).
(4C) Shadow video BIOS ROM.
(4E) If there is any error, show all the error messages on the screen & wait for user to press<F1>. Manufacturing POST loop or display messages; Reboot if manufacturing POST loop pin is set. Otherwise display any messages and enter setup.
(4F) If password is needed, ask for password. Clear the Energy Star logo (Green BIOS only). Security check; Ask password security.
(50) Write all the CMOS values currently in the BIOS stack areas back into the CMOS. Write CMOS; Write all CMOS values back to RAM and clear screen.
(51) Pre-boot enable; Enable parity checker; Enable NMI, Enable cache before boot.
(52) Initialize all ISA ROMs. Later PCI initializations (PCI BIOS only). PnP initializations (PnP BIOS only). Program shadow RAM according to setup settings. Program parity according to setup setting. Power Management initialization. Initialize option ROMs; initialize any option ROMs present from C8000h to EFFFFh.
(53) If it is not a PnP BIOS, initialize serial &parallel ports. Initialize time value in BIOS data area. Initialize time value; Initialize time value in 40h BIOS data area.
(55) Check PCI video Card -or replace video card.
(60) Setup virus protection(Boot sector protection).
(61) Try to turn on level 2 caches. Set the boot up speed according to setup setting. Last chance for chipset initialization. Last chance for power management initialization. Show the system configuration table.
(62) Setup daylight saving according to setup values. Program the NUM lock, type rate & type speed according to setup setting. Setup NUM_LOCK; Setup NUM_LOCK status according to setup.
(63) If there is any changes in the hardware configuration, update the ESCD information n(PnP BIOS only. Clear memory that have been used. Boot system via INT 19h.
(B0) Spurious interrupt occurred in protect mode. Check mismatch memory.
(B1) If unmasked NMI occurs, Press F1 to disable NMI,F2 to boot.
(BE) Program defaults values into chipset.(BE) Chipset default initialization; Program chipset registers with power on BIOS defaults.
(BF) Program the rest of the chipset (BF) Chipset initialization; Program chipset registers with setup values.
(C0) Turn off chipset cache; OEM Specific -cache control.
(C1) Memory presence test; OEM specific-test to size on - board memory. Bad SIMM.
(C3) DRAM Select page, Check BIOS setting and first SIMM, Possible address line failure.
(C4) CMOS conflicts, check video switch, BIOS(Chipset) on the video not initializing.
(C5) Early shadow; OEM Specific -Early shadow enable for fast boot.
(C6) Cache presence test; External cache size detection. (Check Memory first 64K.Check CPU jumper Setting). Also, Check Video memory
(C7) Shadow video/system BIOS after memory pass.
(C8) CMOS Shutdown, time delay.
(CA) Micronics cache initialization.
(CC) NMI handler shutdown.

(FF) System booting. This means that the BIOS already passed control to the operation system. If no error flags such as memory size are set, boot via INT 19 –load system from drive A, then C; display error message if correct boot device not found. Boot system.
(EE) Unexpected Processor exception.

(3) Phoenix

(01) [Beep]=none 80286 register test in progress.
(02) Verify real -mode operation (Beep) =1 -1-1-3.CPU Flags test.
(02) [Beep]=1-1-3 CMOS write/read test in -progress or failure.
(03) Disable Non-Maskable Interrupt (NMI). [Beep]=1-1-4 BIOS ROM checksum in-progress or failure.
(04) Get the CPU type (Beep)=1-1-2-1.CPU register test. Programmable Interval Timer test failure.
(05) [Beep]=1-2-2 DMA initialization in-progress or failure.
(06) Initialize system hardware (Beep) =1-1-2-3.DMA page register write/read test in-progress or fail.
(08) Initialize chipset registers with POST values. [Beep]= 1-3-1 RAM refresh verification in -progress or failure.
(09) Set POST flay.(Beep)=1-1-3-2. 1st 64K RAM test in-progress.
(0A) Initialize CPU registers. (Beep)=1 -1-3-3. Perform BIOS checksum test. 1st 64K RAM chip or data line failure multi -bit.
(0B) Enable CPU Cable -Check CPU Jumpers. [Beep]=1-3-4 1st 64K RAM odd/even logic failure.
(0C) Initialize cache to initial POST value. Test DMA page registers. [Beep]=1-4-1 1st 64K RAM address line failure.
(0D) [Beep]=1-4-2 1st 64K RAM parity test in progress or failure.
(0E) Initialize I/O.(Beep)=1 -1-4-3. Test 8254 timers.
(0F) Initialize the local IDE
(10) Initialize Power Management.(Beep)=1-2-1-1.Initialize 8254 timers.[Beep]=2-1-1 1st 64K RAM chip or data line failure-bit 0.
(11) Load alternate registers with POST values.(Beep)=1-2-2. 1st 64K RAM chip or data line failure-bit 1.
(12) Restore CPU control word during warm boot. J ump to User Path 0.(Beep)=1-2-1-3.Test both 8237 DMA controllers. 1st 64K RAM chip or data line failure-bit 2.
(13) [Beep]=2-1-4 1st 64K RAM chip or data line failure -bit 3. Initialize PCI Bus Mastering devices.
(14) Initialize keyboard controller.(Beep)=1-2-2-1.Initialize 8237 DMA controllers.[Beep]=2 -2-1 1st 64K RAM chip or data line failure -bit 4.
(15) [Beep]=2-2-2 1st 64K RAM chip or data line failure-bit 5.
(16) BIOS ROM checksum.(Beep)=1-2-2-3. Initialize 8259, reset Coprocessor.[Beep]=2-2-3 1st 64K RAM chip or data line failure -bit 6.
(17)Initialize cache before memory auto -size. [Beep] =2-2-4 1st 64K RAM chip or data line failure-bit 7.
(18)8254 timer initialization. (Beep)=1-2-3-1. Test 8259 interrupt controllers registers. [Beep]=2-3-1 1st 64K RAM chip or data line failure -bit 8.
(19) Check memory [Beep] =2-3-2 1st 64K RAM chip or data line failure -bit 9.
(1A) 8237 DMA controller initialization. (Beep)=1-2-3-3. Verify refresh is occurring. [Beep]=2-3-3 1st 64K RAM chip or data line failure-bit A.
(1B) [Beep] =2-4-1 1st 64K RAM chip or data line failure - bit B.
(1C) [Beep] =2 -4-1 1st 64K RAM chip or data line failure-bit C. Reset Programmable Interrupt Controller.(Beep)=1 -2 ¨C4-1.Base 64K address test.
(1D) [Beep] =2-4-2 1st 64K RAM chip or data line failure - bit D.
(1E) [Beep]=2-4-3 1st 64K RAM chip or data line failure - bit E. Base 64K RAM test (16 b its).
(1F) [Beep] =2-4-4 1st 64K RAM chip or data line failure - bi t F.

(20) [Beep] =3-1-1 master DMA register test in -progress or failure. Test DRAM refresh.(Beep)=1-3-1-1. Upper 16 of 32 bit test failed.
(21) [Beep] =3-1-2 slave DMA register test in -progress or failure.
(22) [Beep] =3-1-3 master interrupt mask register test in - progress or fail. Test 8742 keyboard controller.(Beep)=1-3-1-3
(23) [Beep] =3-1-4 slave interrupt mask register test in -progress or fail.
(24) Set ES segment to register to 4 GB. (Beep)=1-3-2-1. Verify CMOS/Configure CMOS.
(25) [Beep] =none interrupt vector loading in-progress.
(26) Enable A20 line. Verify/Load NVRAM parameters.
(27) [Beep] =3-2-4 keyboard controller test in -progress or failure.
(28) [Beep]=3-3-1 CMOS power-fail and checks um checks in-progress. Auto –size DRAM. (Beep)=1 -3-3-1.Protected mode 1.
(29) [Beep] =3-3-2 CMOS configuration info validation in - progress. Initialize POST Memory Manager.
(2A) Clear 512K base RAM.(Beep)=1 -3-3-3.Aubo-site memory chips.
(2B) [Beep]=3 -3-4 screen memory test in-progress or failure.
(2C) RAM failure on address xxxx. If the BIOS detects error 2C,2E,or 30(base 512K RAM error),it displays and additional word –bitmap (xxxx) indication the address line or bits that failed. For example, "2C 0002"means address line 1 (bit one set) has failed. "2E 1020 means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because the y have a
16 rather than 32-bit bus. The BIOS also sends the bitmap to the port -80 LED display. It first display the check point code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.
Test 512 base address lines.(Beep)=1-3-4-1 Activate interleave(if possible).[Beep] 3-4-1 screen initialization in -progress or failure.
(2D) [Beep]=3-4-2 screen retrace tests in -progress or failure.
(2E) See Error code "2C". Test 512K base memory.(Beep)=1-3-4-3. Exit 1st protected mode test.[Beep]=none search for video ROM in -progress.
(2F) Enable cache before system BIOS shadow.
(30) see Error Code "2C".Unexpected shutdown.[Beep]=no - ne screen believed operable. [Beep]=none screen believed running w/video ROM.
(31) [Beep]=none monochromatic screen believed operable.
(32) Test CPU bus-clock frequency.(Beep)=1-4-1-3.Deter- mine system board memory size. [Beep]=none 40-column color screen believed operable.
(33) [Beep]=none 80 -column color screen believed operable. Initialize dispatch Manager.
(34) [Beep]=4-2-1 timer tick interrupt test in progress or failure. Relocate memory option.
(35) [Beep]=4-2-2 shutdown test in progress or failure.
(36) [Beep]=4-2-3 gate A20 failure. Warm start shut down. Configure EMS memory option.
(37) [Beep]=1-4-2-4 unexpected interrupt in protected mode. Reinitialize the motherboard chipset.
(38) [Beep]=4-3-1 RAM test in progress or failure above address 0FFFFh
(38) Shadow system BIOS ROM.(Beep)=1 -4-3-1.Configure wait state option.
(39) Reinitialize the cache.(Beep)=1 -4-3-1
(3A) [Beep]=4-3-3 Interval timer channel 2 test in progress or failure.
(3A) Auto -size cache.(Beep)=1 -4-3-3.Retest 64K base RA M.
(3B) [Beep]=4 -3-4 Time-Of-Day clock test in progress or failure.
(3C) [Beep]=4 -4-2 Serial port test in progress or failure.
(3D) Load alternate registers with CMOS values,(Beep)= 1 -4-4-2
(3D) [Beep]=4-4-2 Parallel port test in progress or failure.
(3E) Get switches/jumper status from 8742.
(3E) [Beep]=4-4-3 Math CoProcessor test in progress or failure.
(40) Set initial CPU speed.(Beep)=2-1-1-1.
(42) Initialize interrupt vectors.(Beep)=2-1-1-3.

(44) Initialize BIOS interrupts.(Beep)=2-1-2-1. Verify video con figuration.
(45) POST device initialization.
(46) Check ROM copying notice.(Beep)=2-1-2-3. Initialize video system.
(47) Initialize manager for PCI Options ROMs.(Beep)=2-1-2-4.
(48) Check Video configuration against CMOS.(Beep)=2-1-3-1. Test for unexpected interrupts.
(49) Initialize PCI bus and devices. (Beep)=2-1-3-2.
(4A) Initialize all video adapters in system. (Beep)=2 -1-3-3. Start 2nd protected mode test.
(4B) Quiet-Boot starts (optional).
(4C) Shadow video BIOS ROM. (Beep)=2 -1 -4-1.Perform LDT instructions test.
(4E) Display copying notice. (Beep)=2 -1-4-3. Perform TR instruction test.
(50) Display CPU type and speed. (Beep)=2 -2-1-1.(50)Per- form LSL instruction test.[Beep]=none Custom chip set or custom platform.
(51) Initialize EISA board.
(52) Test keyboard. (Beep)=2 -2-1-3.(52)Perform LAR instruction test.
(54) Set key click if enabled. (Beep)=2 -2-2-1.(54)Perform VERR instruction test.
(56) Enable keyboard.(Beep)=2-2-2-3.Unexpected exception.
(58)Test for unexpected interrupts. (Beep)=2-3-3-.(58) Perform A20 gate test.
(59) Initialize POST display service.
(5A) Keyboard ready test. Display prompt "press F2 to enter SETUP". (Beep)=2-2-3-3
(5B) Display CPU cache.
(5C) Test RAM between 512 and 640K.(Beep)=2-2-4-1. Determine if AT or KT keyboard type.
(5E) Enter third protected mode test.
(60) Test expanded memory.(Beep)=2-3-1-1.(60)Base memory test.
(62) Test extended memory address lines.(Beep)=2-3-1-3. Base memory address test.
(64) Jump to User Patch 1. (Beep)=2-3-2-1.Shadow memory test.
(67) Initialize Multi Processor APIC.
(68) Enable external and CPU caches.(Beep)=2-3-3-1. Ex- tended address test.
(69) Setup System Management Mode (SMM) area.
(6A) Display external cache size.(Beep)=2-3-3-3.Determine memory test.
(6B) Load custom defaults (optional).
(6C) Display shadow message.(Beep)=2-3-4-1.Display error messages.
(6E) Display possible high address for UMB recovery. Display non-disposable segments. (Beep)=2 -3-4-3.Configure ROM/RAM BIOS.
(70) Display error messages.(Beep)=2-4-1-1.System time test.
(72) Check for configuration errors.(Beep)=2-4-1-3.(72) Real time clock test.
(74) Test real-time clock.(Beep)=2 -4-2-1.Test for stuck keys.
(76) Check for keyboard errors. (Beep)=2-4-2-3.Initialize hardware interrupts vectors.
(78) Detect and test CoProcessor.
(7A) Determine/Init COM channels.
(7C) Set up hardware interrupts vectors.(Beep)=2-4-4-1.Determine LPT channels.
(7E) Test CoProcessor if p resent.(Beep)=2-4-4-3.Initialize BIOS data area.
(80) Disable onboard Super I/O ports and IRQs.(Beep)=3-1-1-1.Detect floppy controller.
(81) late POST device initialization.
(82) Detect and ins tall external RS232 ports. (Beep)=3-1- 1-3.Test floppy drives.
(83) Configure non -MCD IDE controllers.
(84) Detect and install external parallels ports.(Beep)=3-1- 2-1.Fixed disk test.
(85) Initialize PC-compatible PnP ISA devices.
(86) Re-initialize onboard I/O ports.(Beep)=3-1-2-3.(86)Per form external ROM scan.
(87) Configure Motherboard Configuration Devices(option - al)
(88) Initialize BIOS Data Area.(Beep)=3-1-3-1.Test key- lock/keyboard type.
(89) Enable Non - Maskable Interrupts (NMIs)
(8A) Initialize Extended BIOS Data Area.(Beep)=3-1-3-3. wait for F1 test.
(8B) Test and initialize PS/2 mouse.

(8C) Initialize floppy controller.(Beep)=3-1-4-1.Final system initialization.
(8E) Interrupt 19 boot loader.
(8F) Determine number o f ATA drives(optional)
(90) Initialize hard -disk controller.(Beep)=3-2-1-1
(91) Initialize local-bus hard-disk controller.(Beep)=3 -2-1-2
(92) Jump to User Patch 2.(Beep)= 3-2-1-3
(93) Build MPTABLE for multi processor boards.
(94) Disable A20 address line.(Beep)=3-2-2-1
(95) Install CD ROM for boot.
(96) Clear huge ES segment register.(Beep)=3-2-2-3.
(97) Fix-up Multi Processor table.
(98) Search for option ROMs. One long, two short beeps on checksum failure. (Beep)=3 -2-3-1.
(99) Check for SMART Drive (optional).
(9A) Shadow option ROMS. (Beep)=3-2-3-3.
(9C) Set up Power Management.(Beep)=3-2-4-1.
(9E) Enable hardware interrupts.(Beep)=3-2-4-3.
(9F) Determine number at ATA and SCSI drives.
(A0) Set time of day. (Beep)=3-3-1-1
(A2) Check key lock.(Beep)=3-3-1-3
(A4) Initialize Type matri crate.
(A8) Erase F2 prompt.(Beep)3-3-3-1
(AA) Scan for F2 key stroke.(Beep)=3-3-3-3
(AC) Enter SETUP. (Beep)=3-3-4-1
(AE) Clear in-POST flag.(Beep)=3-3-4-3.Clear Boot fag.
(B0) Check for errors.(Beep)=3-4-1-1.Unknown interrupt occurred.
(B2) POST done-prepare to boot operating system.(Beep)=3-4-1-3
(B4) One short beep before boot.(Beep)=3-4-3-1
(B5) terminate Quiet -Boot (optional)
(B6) Check password (optional). (Beep)=3-4-2-3
(B8) Clear global descriptor table.(Beep)=3-4-3-4
(B9) Prepare boot.
(BA) Initialize DMI parameters.
(BB) Initialize PnP option ROMs.
(BC) Clear parity checkers.(Beep)=3 -4-4-1
(BD) Display Multi -Boot menu.
(BE) Clear screen(optional).(Beep)=3 -4-4-3
(BF) Check virus and backup reminders.(Beep)=3 -4-4-4
(C0) Try to boot with INT 19.(Beep)=4 -1-1-1
(C1) Initialize POST Error Manager(PEM).
(C2) Initialize error logging.
(C3) Initialize error display function.
(C4) initialize system error handler.
(C5) PnPnd dual CMOS(optional)
(C6) Initialize notebook docking (optional).
(C7) Initialize notebook docking late.
(C8) Force check(optional)
(C9) Extended checksum(optional)
(D0) Interrupt handler error.(Beep)=4-2-1-1
(D2) Unknown interrupt error.(Beep)=4-2-1-3
(D4) Pending interrupt error.(Beep)=4-2-2-1
(D6) Initialize option ROM error.(Beep)4-2-2-3.Shutdown error.(Beep)=4-2-3-1.
(DA) Extended Block Move.(Beep)=4-2-3-3.(DC)Shutdown 10 error(Beep)=4-2-4-1
(E0) Initialize the chipset.

(E1) Initialize the bridge.
(E2) Initialize the motherboard chipset, and CPU.(Beep)=4 -3 -1-3
(E3) Initialize refresh counter and system timer(Beep)=4 -3- 1 ¯C4
(E4) Check for forced Flash or initialize system I/O.(Beep)= 4 -3-2.
(E5) Check HW status of ROM or check force recovery boot.(Beep)4 -3-2-2.
(E6) BIOS ROM is OK. (Beep) =4-3-2-3.
(E7) Do a complete RAM Test or go to BIOS. (Beep)=4 -3-2-4.
(E8) Do OEM initialization or set huge segment. (Beep)=4 -3-3-1.
(E9) Initialize interrupt controller or initialize multi processor. (Beep)=4-3-3-2.
(EA) Read in bootstrap code or initialize OEM special code. (Beep)=4 -3 -3-3.
(EB) Initialize all vectors or initialize PIC and DMA. (Beep)=4 -3-3-4.
(EC) Boot the Flash program or initialize memory type. (Beep)=4-3-4-1.
(ED) Initialize the boot device or initialize memory size. (Beep)=4 -3-4-2
(EE) Boot code was read OK or shadow boot block.(Beep)= 4 -3-4-3
(F0) Initialize interrupt vectors.
(F1) Initialize Run Time Clock.
(F2) Initialize video.
(F3) Initialize System Management Mode.
(F4) Output one beep before DOS.
(F5) Boot to Mini DOS.(F6)Clear Huge Segment.(F7)Boot to Full DOS.

8. Description of beep code

(1). AMI BIOS beep codes (fatal error)

1 beep	DRAM Refresh Failure. Try reseating the memory first. If the error still occurs, replace the memory with known good chips.
2 beeps	Parity Error in First 64K RAM. Try reseating the memory first. If the error still occurs, replace the memory with known good chips.
3 beeps	Base 64K RAM Failure. Try reseating the memory first. If the error still occurs, replace the memory with known good chips.
4 beeps	System timer failure
5 beeps	Process failure
6 beeps	Keyboard Controller 8042 - Gate A20 Error. try reseating the keyboard controller chip. If the error still occurs, replace the keyboard chip. If the error persists, check parts of the system relating to the keyboard, e.g. try another keyboard, check to see if the system has a keyboard fuse
7 beeps	Processor Virtual Mode Exception Interrupt Error
8 beeps	Display Memory Read/Write Test Failure (Non-fatal). Replace the video card or the memory on the video card.
9 beeps	ROM BIOS Checksum (32KB at F800:0) Failed. It is not likely that this error can be corrected by reseating the chips. Consult the motherboard supplier or an AMI product distributor for replacement part(s).
10 beeps	CMOS Shutdown Register Read/Write Error
11 beeps	Cache memory error

(2). AMI BIOS beep codes (Non-fatal error)

2 short	POST Failure - One or more of the hardware tests has failed
1 long 2 short	An error was encountered in the video BIOS ROM, or a horizontal retrace failure has been encountered
1 long 3 short	Conventional/Extended memory failure
1 long 8 short	Display/Retrace test failed

(3). Award BIOS beep codes

1 short	No error during POST
2 short	Any Non-fatal error, enter CMOS SETUP to reset
1 long 1 short	RAM or motherboard error
1 long 2 short	Video Error, Cannot Initialize Screen to Display Any Information
1 long 3 short	Keyboard Controller error
1 long 9 short	Flash RAM/EPROM (which on the motherboard) error. (BIOS error)
Long beep	Memory bank is not plugged well, or broken.

(4). Phoenix BIOS beep codes

Beep Code	Description / What to Check	Beep Code	Description / What to Check
1-1-1-3	Verify Real Mode.	2-4-1-3	Check for configuration errors.
1-1-2-1	Get CPU type.	2-4-2-1	Test real-time clock.
1-1-2-3	Initialize system hardware.	2-4-2-3	Check for keyboard errors
1-1-3-1	Initialize chipset registers with initial POST values.	2-4-4-1	Set up hardware interrupts vectors.
1-1-3-2	Set in POST flag.	2-4-4-3	Test coprocessor if present.
1-1-3-3	Initialize CPU registers.	3-1-1-1	Disable onboard I/O ports.
1-1-4-1	Initialize cache to initial POST values.	3-1-1-3	Detect and install external RS232 ports.
1-1-4-3	Initialize I/O.	3-1-2-1	Detect and install external parallel ports.
1-2-1-1	Initialize Power Management.	3-1-2-3	Re-initialize onboard I/O ports.
1-2-1-2	Load alternate registers with initial POST values.	3-1-3-1	Initialize BIOS Data Area.
1-2-1-3	Jump to UserPatch0.	3-1-3-3	Initialize Extended BIOS Data Area.
1-2-2-1	Initialize keyboard controller.	3-1-4-1	Initialize floppy controller.
1-2-2-3	BIOS ROM checksum.	3-2-1-1	Initialize hard-disk controller.
1-2-3-1	8254 timer initialization.	3-2-1-2	Initialize local-bus hard-disk controller.
1-2-3-3	8237 DMA controller initialization.	3-2-1-3	Jump to UserPatch2.
1-2-4-1	Reset Programmable Interrupt Controller.	3-2-2-1	Disable A20 address line.
1-3-1-1	Test DRAM refresh.	3-2-2-3	Clear huge ES segment register.
1-3-1-3	Test 8742 Keyboard Controller.	3-2-3-1	Search for option ROMs.
1-3-2-1	Set ES segment to register to 4 GB.	3-2-3-3	Shadow option ROMs.
1-3-3-1	28 Autosize DRAM.	3-2-4-1	Set up Power Management.
1-3-3-3	Clear 512K base RAM.	3-2-4-3	Enable hardware interrupts.
1-3-4-1	Test 512K base address lines.	3-3-1-1	Set time of day.
1-3-4-3	Test 512K base memory.	3-3-1-3	Check key lock.
1-4-1-3	Test CPU bus-clock frequency.	3-3-3-1	Erase F2 prompt.

1-4-2-4	Reinitialize the chipset.	3-3-3-3	Scan for F2 key stroke.
1-4-3-1	Shadow system BIOS ROM.	3-3-4-1	Enter SETUP.
1-4-3-2	Reinitialize the cache.	3-3-4-3	Clear in-POST flag.
1-4-3-3	Auto size cache.	3-4-1-1	Check for errors
1-4-4-1	Configure advanced chipset registers.	3-4-1-3	POST done--prepare to boot operating system.
1-4-4-2	Load alternate registers with CMOS values.	3-4-2-1	One beep.
2-1-1-1	Set Initial CPU speed.	3-4-2-3	Check password (optional).
2-1-1-3	Initialize interrupt vectors.	3-4-3-1	Clear global descriptor table.
2-1-2-1	Initialize BIOS interrupts.	3-4-4-1	Clear parity checkers.
2-1-2-3	Check ROM copyright notice.	3-4-4-3	Clear screen (optional).
2-1-2-4	Initialize manager for PCI Options ROMs.	3-4-4-4	Check virus and backup reminders.
2-1-3-1	Check video configuration against CMOS.	4-1-1-1	Try to boot with INT 19.
2-1-3-2	Initialize PCI bus and devices.	4-2-1-1	Interrupt handler error.
2-1-3-3	Initialize all video adapters in system.	4-2-1-3	Unknown interrupt error.
2-1-4-1	Shadow video BIOS ROM.	4-2-2-1	Pending interrupt error.
2-1-4-3	Display copyright notice.	4-2-2-3	Initialize option ROM error.
2-2-1-1	Display CPU type and speed.	4-2-3-1	Shutdown error.
2-2-1-3	Test keyboard.	4-2-3-3	Extended Block Move.
2-2-2-1	Set key click if enabled.	4-2-4-1	Shutdown 10 error.
2-2-2-3	56 Enable keyboard.	4-3-1-3	Initialize the chipset.
2-2-3-1	Test for unexpected interrupts.	4-3-1-4	Initialize refresh counter.
2-2-3-3	Display prompt "Press F2 to enter SETUP".	4-3-2-1	Check for Forced Flash.
2-2-4-1	Test RAM between 512 and 640k.	4-3-2-2	Check HW status of ROM.
2-3-1-1	Test expanded memory.	4-3-2-3	BIOS ROM is OK.
2-3-1-3	Test extended memory address lines.	4-3-2-4	Do a complete RAM test.
2-3-2-1	Jump to UserPatch1.	4-3-3-1	Do OEM initialization.
2-3-2-3	Configure advanced cache registers.	4-3-3-2	Initialize interrupt controller.
2-3-3-1	Enable external and CPU caches.	4-3-3-3	Read in bootstrap code.
2-3-3-3	Display external cache size.	4-3-3-4	Initialize all vectors.
2-3-4-1	Display shadow message.	4-3-4-1	Boot the Flash program.
2-3-4-3	Display non-disposable segments.	4-3-4-2	Initialize the boot device.
2-4-1-1	Display error messages.	4-3-4-3	Boot code was read OK.

(5). IBM BIOS beep codes

Beep Code	Description
No Beeps	No Power, Loose Card, or Short.
1 Short Beep	Normal POST, computer is ok.
2 Short Beep	POST error, review screen for error code.